WHAT IS CLAIMED IS:

1. A method for boundary detection in a stream of digital sample values, the method comprising:

receiving the stream of digital sample values;

correlating a digital sample value with a plurality of received digital sample values;

calculating a correlation value based on the correlation;

comparing the correlation value against a threshold; and

determining the presence of the boundary based on the comparison.

2. The method of claim 1, wherein the plurality of received digital sample values are selected from the received stream based on their position in different periods of a periodic sequence.

3. The method of claim 1, wherein the received stream is stored in a memory, wherein the boundary being detected is a boundary at an end of a periodic sequence, and wherein the plurality of received digital sample values are digital sample values stored in memory locations with memory addresses that correspond to integer multiples of a number of digital sample

values in a period of the periodic sequence starting at the memory address of the memory location containing the digital sample value.

4. The method of claim 3, wherein the number of digital sample values in the plurality of received digital sample values is less than or equal to the number of periods in the periodic sequence.

5. The method of claim 3, wherein the plurality of received sample values are sample values stored in memory locations that are $N * 2^n$ memory locations from the memory location containing the digital sample value, where n and N are integer values and 2^n is the period of the periodic sequence.

6. The method of claim 5, wherein the plurality of received sample values are sample values stored in memory locations that are 2^n, $2 * 2^n$, $3 * 2^n$, and $4 * 2^n$ memory locations from the memory location containing the digital sample value.

7. The method of claim 6, wherein the digital sample value is stored at a first memory location and the plurality of received sample values are stored at memory locations 2^n + the first memory location, $2 * 2^n$ + the first memory

location, $3 * 2^n$ + the first memory location, and $4 * 2^n$ + the first memory location.

8. The method of claim 6, wherein the digital sample value is stored at a first memory location and the plurality of received sample values are stored at memory locations 2^n - the first memory location, $2 * 2^n$ - the first memory location, $3 * 2^n$ - the first memory location, and $4 * 2^n$ - the first memory location.

9. The method of claim 1, wherein the received stream is stored in memory, and wherein the correlating step comprises:

comparing the digital sample value with the plurality of received digital sample values;

generating a one value for each time the digital sample value matches with one of the digital sample values in the plurality; and

generating a zero value for each time the digital sample value does not match with one of the digital sample values in the plurality.

10. The method of claim 1, wherein the calculating step comprises summing up a correlation result resulting from each correlation of the digital sample value with the plurality of previously received digital sample values.

11. The method of claim 1, wherein the threshold is a predetermined value.

12. The method of claim 1, wherein the threshold is adaptive and its value can change depending on network conditions.

13. The method of claim 1, wherein the boundary detection is performed after each sample value is received.

14. The method of claim 1, wherein the boundary detection is performed after a specified number of sample values is received.

15. A circuit for detecting boundaries in a stream of digital sample values, the circuit comprising:

a memory for storing at least a portion of the stream of digital sample values;

a plurality of comparators coupled to the memory, a first input of each comparator coupled to a single memory location and a second input of each comparator coupled to different memory locations wherein the different memory locations correspond to digital sample values that are desired to be compared to a digital sample value stored in the single memory location, each comparator configured to output a one value if the comparison is equal and a zero vale if the comparison is not equal; and

a summing circuit coupled to the plurality of comparators, the summing circuit containing circuitry to add the outputs from the plurality of comparators and produce a correlation value.

16. The circuit of claim 15, wherein the circuit is configured to generate a correlation value after the receipt of each digital sample value.

17. The circuit of claim 15, wherein the circuit is configured to generate a correlation value after the receipt of a specified number of digital sample values.

18. The circuit of claim 15, wherein the memory is sized sufficiently to at least store the digital samples being correlated.

19. The circuit of claim 15, wherein the comparators will output a one value if the digital samples being compared are within a specified difference of each other and the comparator will output a zero value if the digital samples being compared are outside of a specified difference of each other.

20. The circuit of claim 15, wherein the memory location stores more than one digital sample.

21. A station in a communications network, the station comprising:

a transceiver to transmit and receive information being sent to and from the station;

a transmit path coupled to the transceiver, the transmit path containing circuitry to convert information from the station into a form suitable for transmission;

a receive path coupled to the transceiver, the receive path containing circuitry to convert information sent to the station into a form suitable for use; and

a processor coupled to the transmit and receive paths, the processor containing circuitry to detect boundaries in a stream of digital sample values, the processor comprising:

a memory for storing at least a portion of the stream of digital sample values;

a plurality of comparators coupled to the memory, a first input of each comparator coupled to a single memory location and a second input of each comparator coupled to different memory locations wherein the different memory locations correspond to digital sample values that are desired to be compared to a digital sample value stored in the single memory location, each comparator configured to output a one value if the comparison is equal and a zero vale if the comparison is not equal; and

a summing circuit coupled to the plurality of comparators, the summing circuit containing circuitry to add the outputs from the plurality of comparators and produce a correlation value.

22. The station of claim 21, wherein the station is part of a wireless communications network.

23. The station of claim 21, wherein the station is part of a wired communications network.

24. The station of claim 21, wherein the station is part of a hybrid wired/wireless communications network.